## REMARKS

As a preliminary matter, it is noted that box 2a of the Office Action Summary indicates that the outstanding Office Action is final whereas the last four lines of page 8 of the outstanding Office Action indicates it is non-final. In order to clarify this issue, Applicants' representative contacted the Examiner during which discussion the Examiner confirmed that the outstanding Office Action is non-final. Indeed, the new grounds of rejection presented in the outstanding Office Action were not necessitated by any amendment. Accordingly, it is respectfully that the enclosed amendment/response be treated as a response to a non-final Office Action so as to be entered and fully considered. Applicants and Applicants' representative would like to thank the Examiner for his courtesy in providing the clarification.

Claims 1-11 stand rejected under 35 U.S.C. § 101 as allegedly being non-statutory. It is respectfully submitted that this issue has been obviated by the enclosed amendment. Accordingly, it is respectfully submitted that this rejection be withdrawn.

Claims 1-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith et al. '714 ("Smith") in view of Yonezawa et al. '802 ("Yonezawa"). Claims 1-11 have been canceled rendering this rejection moot.

Claims 12-21 have been added and are submitted to be patentable over the cited prior art. Claim 12 is the sole independent claim. Indeed, it is respectfully submitted that the cited prior art fails to disclose or suggest at least several of the limitations now recited in claim 12.

For example, claim 12 recites in pertinent part, "selecting ... a parameter suitable for each of the transistors provided in the integrated circuit from among the parameters having the model parameter groups according to the stress to carry out a circuit simulation in consideration of a stress applied to each of the transistors." On the other hand, Smith is directed to an arrangement of dummy fill when forming wirings using a CMP process (*see, e.g.,* Figs. 7, 15 and 16), so as to be completely different from the present invention let alone suggest the aforementioned feature of the present invention.

Yonezawa similarly fails to disclose or suggest the features now recited in claim 12. That is, Yonezawa is directed to a method of obtaining a suitable amount of an aging deterioration margin that should be taken into account when designing or inspecting an LSI, by predicting characteristic degradation of the LSI caused with time by the hot carrier degradation, for instance. As shown in Fig. 5, Yonezawa predicts a delay deterioration rate from the LSI design information. Indeed, the unit circuit stress calculating part 111b of Yonezawa (shown in Fig. 5) calculates a stress applied to a unit circuit such as a transistor. On the other hand, the present invention can obtain device measurement data by measuring an electrical characteristic of a device for measurement in which transistors each having a different stress are provided, and convert the device measurement data into parameters having model parameter groups according to the stress so as to make it possible for the parameters to be used for a circuit simulation.

Accordingly, neither Smith nor Yonezawa, alone or in combination, disclose or suggest each and every feature of the claimed ***combination*** set forth in claim 12.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a

single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that the cited prior art does not anticipate claim 12, nor any claim dependent thereon. The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard for establishing obviousness under § 103:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the cited prior art does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 12 because the cited prior art fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 12 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 103 be withdrawn.

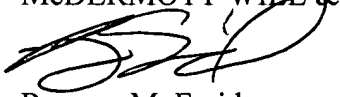
## CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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